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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,004	10/18/2000	Leonard Forbes	303.324US4	4509

7590 09/30/2004

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,004	FORBES ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-39,59-61,71-85,98 and 99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-39,59-61,83-85,98 and 99* is/are allowed.

6)☒ Claim(s) *71-82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 10, 2004 has been entered.

Response to Amendment

Amendment filed as After-Final Amendment July 22, 2004, has been entered following aforementioned Request for Continued Examination forms the basis of this official action. In said Amendment Applicant substantially amended claims 36, 37, 38, 71, 74, 77 and 80. Claims 36-39, 59-61, 71-85 and 98-99 are pending in the application, claims 1-35, 40-58, 62-70, 86-97 and 100 having been canceled. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 71, 73, 74, 76, 77, 79, 80 and 82*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al (4,507,673). Aoyama et al teach (cf. Fig. 6 and

cols. 2 –5) a floating gate transistor (cf. col. 2, l. 35-38 and col. 5, l. 7-8) comprising: a source region 2 (cf. col. 2, l. 41) formed in a substrate 1 (cf. col. 2, l. 40); a drain region 3 (cf. col. 2, l. 41) formed in the substrate; a channel region in the substrate between the source region and the drain region (inherently a channel is interposed between source and drain in a FET); a floating gate 5 (cf. col. 2, l. 46 and col. 5, l. 6-11; N.B.: "insulating film" 5 is a floating gate because it traps charges: see col. 3, l. 30-34; see also col. 5, l. 6-16) separated from the channel region by an insulator 4 (cf. col. 2, l. 47), the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be x=0.5, i.e., a limit point of the claimed range; and a control gate 7 (cf. col. 2, l. 50-57) (see gate lead wire 10 connected to 7) and separated from the floating gate by an intergate dielectric 41 (cf. col. 5, l. 6-25). Aoyama et al do not teach the range for x according to either of the claims 71, 74, 77 or 80. However, the value selected by Aoyama et al is a limit point of each of the ranges according said claims 71, 74, 77 and 80. Applicants, in their disclosure, do not show why the difference between the claimed ranges and the value x=0.5, in particular, why the difference between x=0.5 and any x infinitesimally greater (for claims 71 and 80) or smaller (for claims 74 and 77) than x=0.5 is critical to their invention. Applicants are reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

With regard to claims 73, 76, 79 and 82: Aoyama et al teach said floating gate to comprise a material that necessarily includes carbide of sizable crystals (see annealing step, col. 4, l. 17-21), while furthermore the group of monocrystalline silicon carbide, polycrystalline silicon carbide, microcrystalline silicon carbide and nanocrystalline silicon carbide includes all forms of silicon carbide because the interatomic distance of silicon carbide is in the nanometer range (see any text book, such as S.M. Sze, "Physics of Semiconductor Devices", second edition, Appendix F). Therefore, the further limitations of claims 73, 76, 79 and 82 do not distinguish over the prior art.

4. ***Claims 72, 75, 78 and 81*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al (4,507,673) in view of Parris et al (5,604,700).

As detailed above, claims 71, 74, 77 and 80 are unpatentable over Aoyama et al. Although Aoyama et al teach the insulator 4 to comprise silicon dioxide (cf. col. 2, l. 42) and also claim said substrate to be a semiconductor substrate of a first conductivity type, said source and drain regions to be of second conductivity type (cf. col. 6, claim 1) both being formed in said substrate, Aoyama et al do not specifically teach (a) said first conductivity and second conductivity types to be p-type and n-type conductivity types, respectively, nor (b) said integrate dielectric to comprise silicon dioxide. However, it would have been obvious to include limitation ad (a) in view of Parris et al, who, in a patent on a non-volatile memory cell with floating gate (cf. title), hence analogous art, teach the application of EEPROM technology to CMOSFETs, in which two transistors, i.e., PMOS transistor 11 and NMOS transistor 12 (cf. abstract and Figures 1 and 4)

share a common floating gate 13 (cf. abstract). Limitation ad (a) is thus met by a mere application of EEPROM to CMOS devices using advantageously a single deposition for the construction of the floating gate (cf. col. 1, l. 1-67). With regard to the limitation ad (b), Parris et al also teach the dielectric layer 54 (cf. Figure 4 and col. 5, l. 52-56) to be made of silicon dioxide thus providing a complete surrounding by silicon dioxide of the floating gate 46 (cf. Figure 4) at least for the purpose of stress relief through doping (cf. col. 5, l. 52-56). In summary, *motivation* to include the teachings ad (a) and (b) in this regard by Parris et al in the invention by Aoyama et al derives from the efficient manufacture of a CMOS EEPROM device through a single floating gate and efficient relief from material stress. *Combination* of said teaching with said invention is straightforward through a mere application of floating gate technology to CMOS transistors and the selection of the very same dielectric material for element 41 as already selected for element 4 in Aoyama et al.

Allowable Subject Matter

5. ***Claims 36-39, 59-61, 83-85 and 98-99*** are allowed. The following is a statement of reasons for the indication of allowable subject matter:

(a) With regard to claims 36, 38, 39 and 98: within the context of the transistor otherwise defined by claim 36, neither Halvis et al nor Chiang et al nor any other reference previously cited, teach the stoichiometry parameter x to be substantially greater than 0.5. No other prior art has come to light in this regard.

(b) With regard to claims 37 and 99: within the context of the transistor otherwise defined by claim 37, neither Weitzel, Halvis et al nor Chiang et al, nor any other

reference previously cited, teach the stoichiometry parameter x to be greater than 0.6. No other prior art has come to light in this regard.

(c) With regard to claims 59-61: within the context of the transistor otherwise defined by claim 59, neither Halvis et al nor Chiang et al nor any other reference previously cited, teach the stoichiometry parameter x to be selected between 0.75 and 1.0. No other prior art has come to light in this regard.

(d) With regard to claims 83-85: a floating gate transistor with source, drain, channel and gate insulator with floating gate and control gate is in the prior art (Nakamura et al, loc.cit.). However, the limitation that the floating gate material comprises a silicon carbide compound $Si_{1-x}C_x$ wherein x is selected between 0.75 and 1.0 has not been found (the closest value for the stoichiometric parameter x found in the prior art was a limit point of 0.5). None of the previously cited references teach said limitation. No other prior art has come to light in this regard.

Response to Arguments

6. Applicant's arguments filed 07/22/2004 have been fully considered but they are not completely persuasive. Although the substantial amendments to independent claims 36, 37 and 59 have resulted in allowable subject matter with regard to the relevant claims, claims 71-82 still stand as rejected because of the teaching of x=0.5, which is a limit point of all claimed ranges, as reflected in the rejections overleaf.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Baker et al (4,852,062).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
September 27, 2004

Patent Examiner:

Johannes Mondt
Art Unit: 2826